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Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications
(V) Final Specifications

Module	**14.1" WXGA Color TFT-LCD with LED Backlight design**
Model Name	B141EW05 V5 (Dell P/N: 2H7P2)
Note ( )	***LED Backlight with driving circuit design***

Customer	**Date**	**Approved by**	**Date**
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Note: This Specification is subject to change without notice.

NBBU Marketing Division / AU Optronics corporation

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Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2009/07/14	All	First Edition for Customer		
0.2 2010/01/29	P. 6	TBD	Update Chromaticity Coodinates	
1.0 2010/02/12	P.27-28 P.32-35	Old 2D drawing X31 EDID	New 2D drawing w/ WWAN solution A00 EDID	
1.1 2010/11/22	P.29	Shipping label	New shipping label for Pol 25%	

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1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. High voltage is supplied to these parts when power turn on.

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2. General Description

B141EW05 V5 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. The input signals are eDP interface compatible.

B141EW05 V5 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Specification

The following items are characteristics summary on the table at 25 ℃ condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	357.7 (14.1W")			
Active Area	[mm]	303.36 X 189.6			
Pixels H x V		1280x3(RGB) x 800			
Pixel Pitch	[mm]	0.237			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I_{LED}=20mA) Note: I_{LED} is LED current	[cd/m^2]	220 typ. (5 points average) 200 min. (5 points average) (Note1)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		500:1 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	5.1 max. (Include Logic and Blu power) (Note1)			
Weight	[Grams]	375 max.			
Physical Size **without inverter, bracket.**	[mm]		Min.	Typ.	Max.
		Length	319	319.5	320
		Width	206	206.5	207
		Thickness	-	-	5.5
Electrical Interface		1 channel Display Port			
Surface Treatment		Anti-Glare,			

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Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +65
RoHS Compliance		RoHS Compliance

Note 1. Total power consumption including LED power efficiency <4.9W max.

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I_{LED}=20mA		5 points average	200	220	-	cd/m^2	1, 4, 5.
Viewing Angle	θ_R	Horizontal (Right) CR = 10	40	45	-	degree	4, 9
	θ_L	(Left)	40	45	-		
	ϕ_H	Vertical (Upper) CR = 10	15	20	-		
	ϕ_L	(Lower)	30	40	-		
Luminance Uniformity	δ_{5P}	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	δ_{13P}	13 Points	-	-	1.50		2, 3, 4
Contrast Ratio	CR		400	500	-		4, 6
Cross talk	%				4		4, 7
Response Time	T_r	Rising	-	6	-	msec	4, 8
	T_f	Falling	-	2	-		
	T_{RT}	Rising + Falling	-	8	16		
Color / Chromaticity Coodinates	Red x	CIE 1931	0.570	0.600	0.630		4
	Red y		0.310	0.340	0.370		
	Green x		0.285	0.315	0.345		
	Green y		0.520	0.550	0.580		
	Blue x		0.125	0.155	0.185		
	Blue y		0.115	0.145	0.175		
	White x		0.283	0.313	0.343		
	White y		0.299	0.329	0.359		
NTSC	%		-	45	-		

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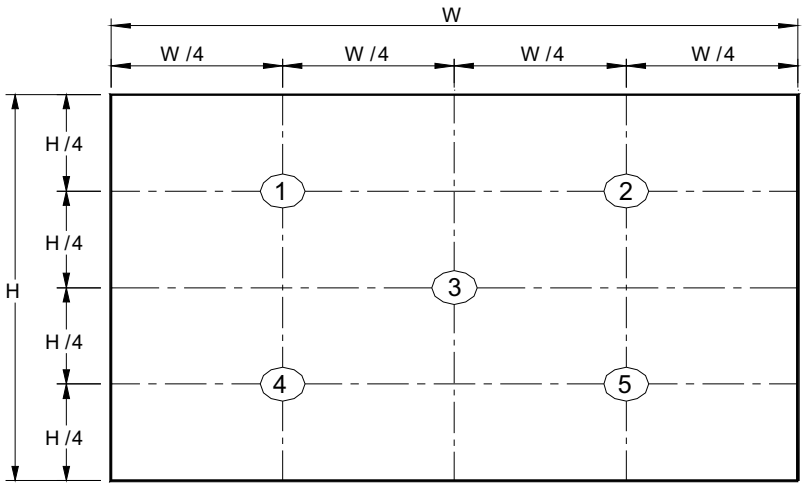
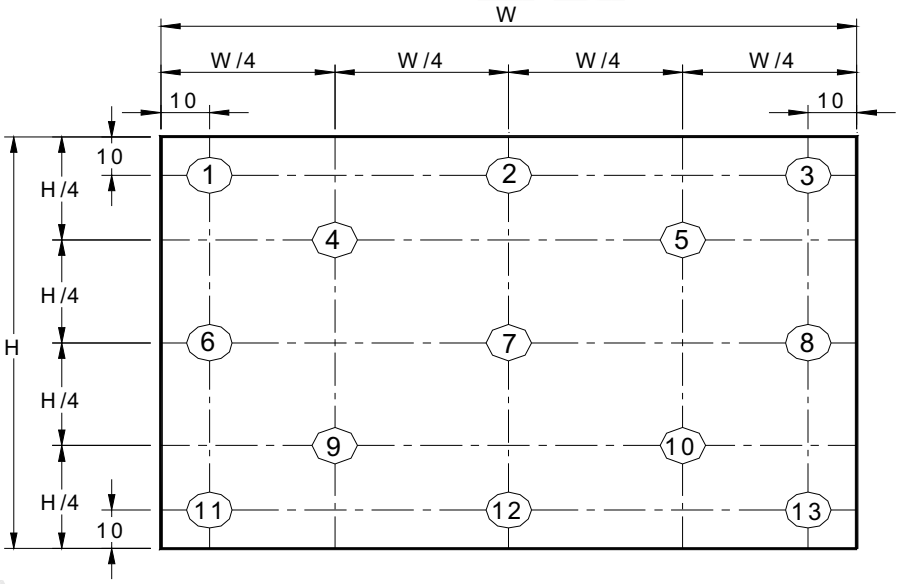
Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

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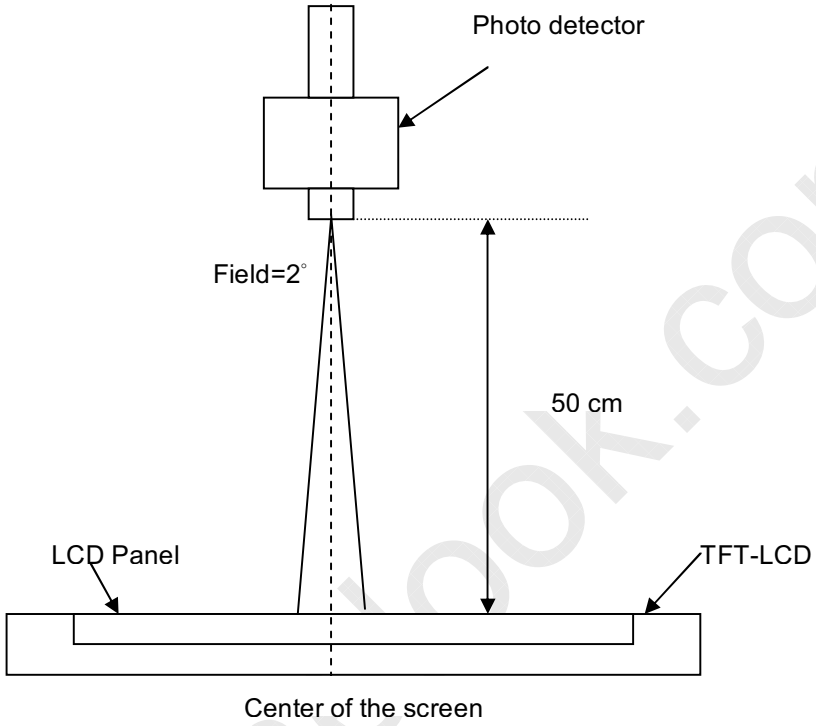
The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, , and it should be measured in the center of screen.



Note 5： Definition of Average Luminance of White (Y_L):

Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6： Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

Note 7： Definition of Cross Talk (CT)

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

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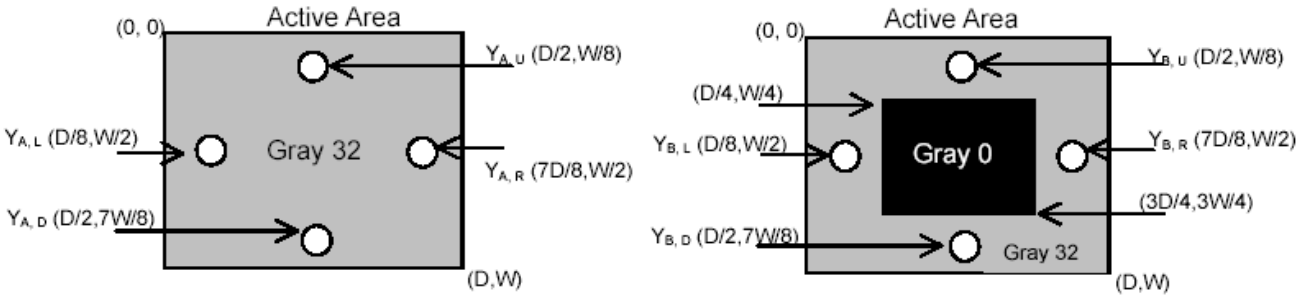
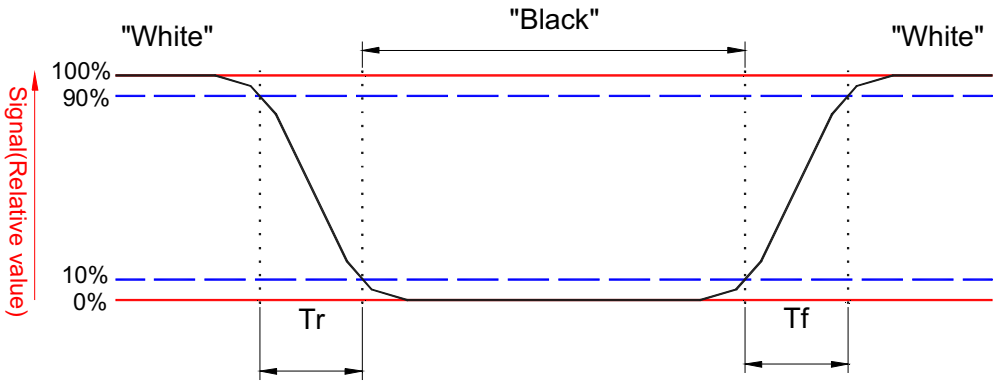
Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



Note 8: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



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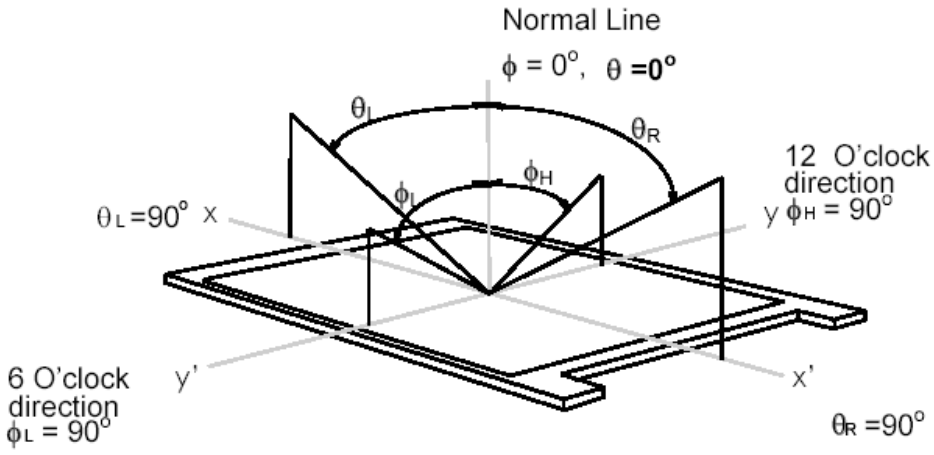
Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180°horizontal an d 180° vertical range (off-normal viewing angles). The 180°viewing angle range is broken down as follows; 90 °(θ) horizontal left and right and 90°(Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



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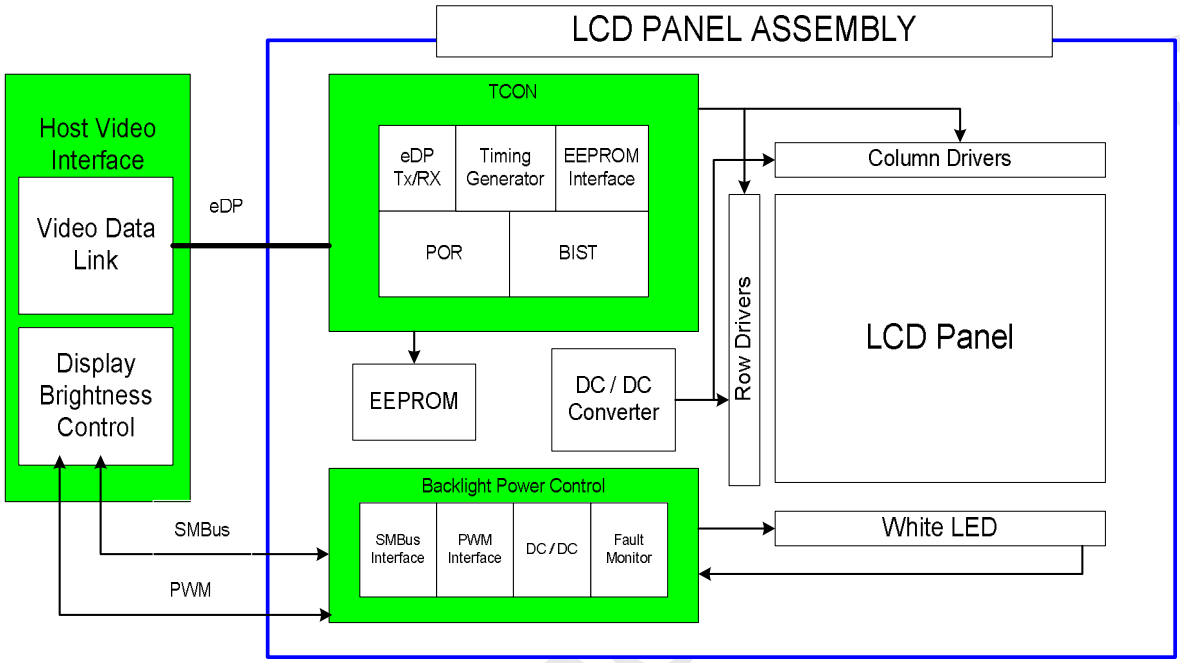
3. Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches wide Color TFT/LCD 30 Pin (One ch/connector Module:



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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

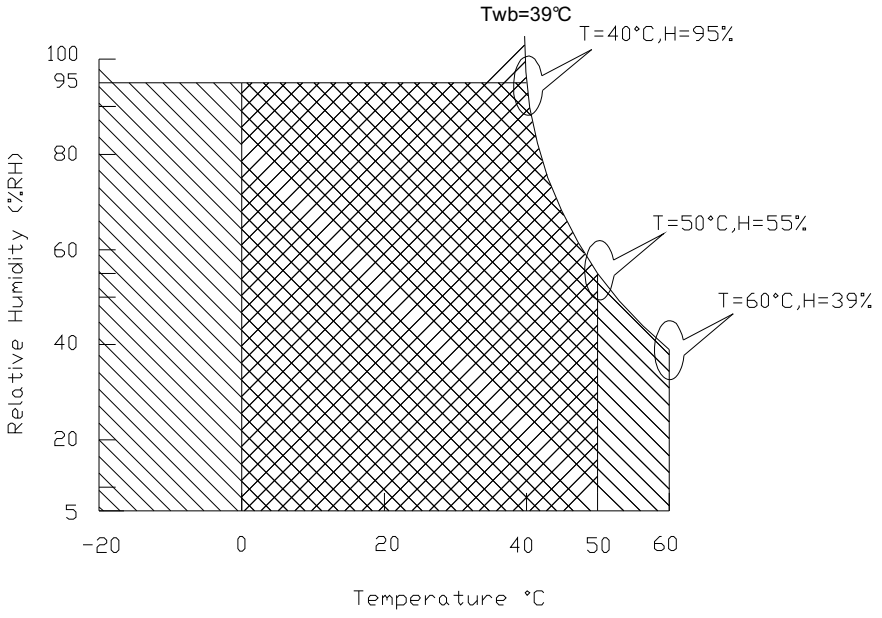
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	8	95	[%RH]	Note 4
Storage Temperature	TST	-20	+65	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

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5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

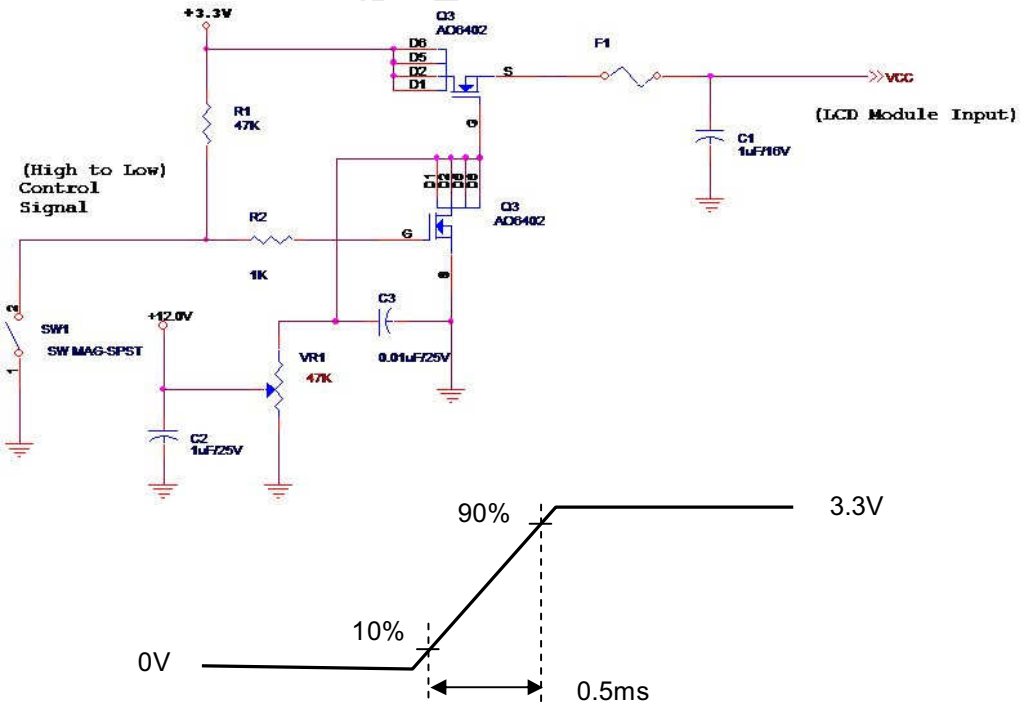
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	1.6	[Watt]	Note 1/2
IDD	IDD Current	-	-	450	[mA]	Note 1/2
IRush	Inrush Current	-	-	2000	[mA]	Note 3
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern

Note 2：Typical Measurement Condition: Mosaic Pattern

Note 3：Measure Condition



Vin rising time

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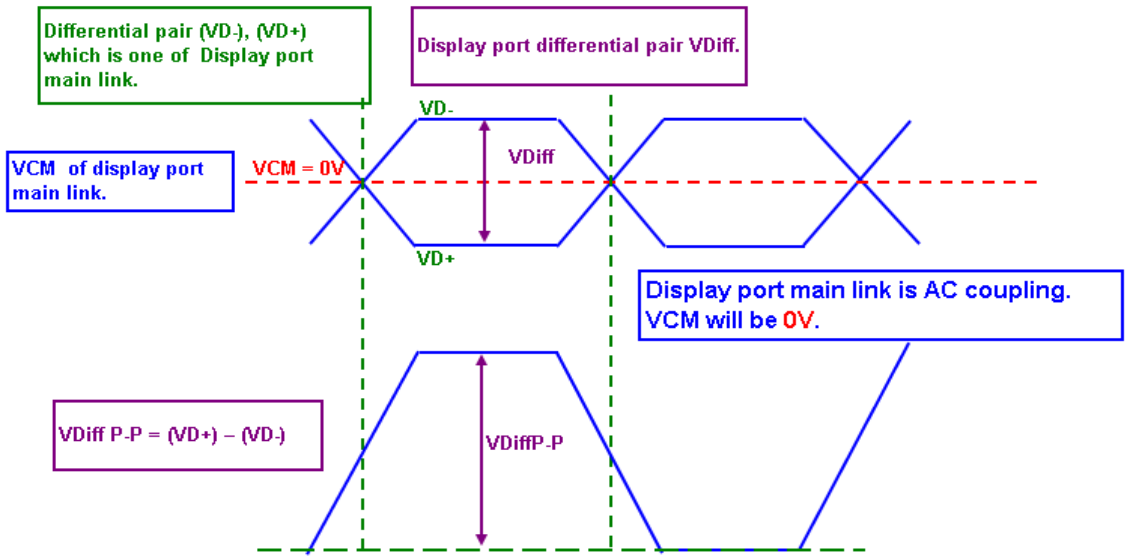
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of VESA Display Port Standard V1.1a (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Display Port main link signal:



Display Port main link					
		Min	Typ	Max	unit
VCM	Differential common mode voltage	TBD	0	TBD	V
VDiffP-P level1	Differential peak to peak voltage level1	0.34	0.4	0.46	V
VDiffP-P level2	Differential peak to peak voltage level2	0.51	0.6	0.68	V
VDiffP-P level3	Differential peak to peak voltage level3	0.69	0.8	0.92	V
VDiffP-P level4	Differential peak to peak voltage level4	1.02	1.2	1.38	V

Fallow as VESA display port standard V1.1a at both 1.62 and 2.7Gbps link rates.

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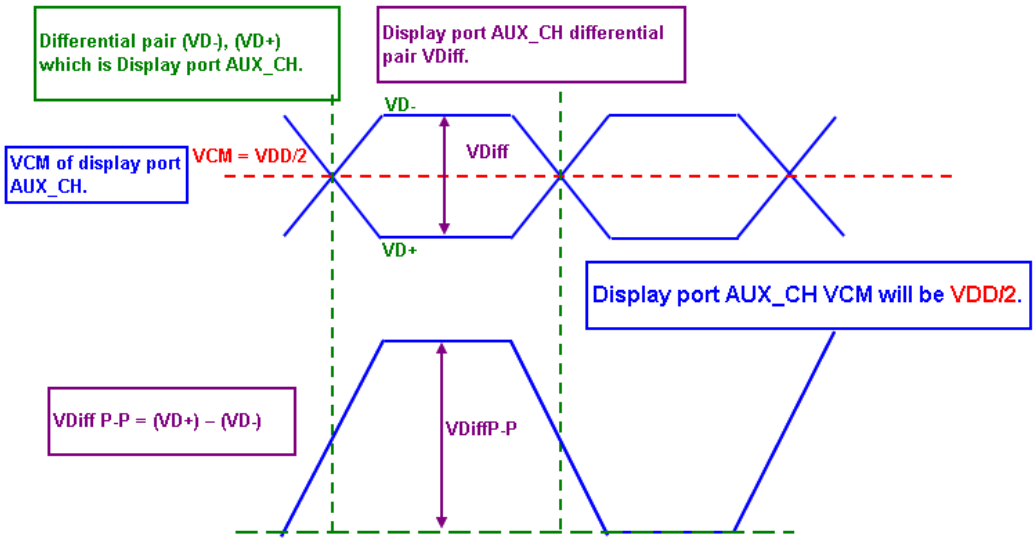
Display Port AUX_CH signal:



Display Port AUX_CH					
		Min	Typ	Max	unit
VCM	Differential common mode voltage	0	VDD/2	2	V
VDiffP-P	Differential peak to peak voltage	0.39		1.38	V

Fallow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display Port VHPD					
		Min	Typ	Max	unit
VHPD	HPD voltage	2.25		3.6	V

Fallow as VESA display port standard V1.1a.

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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.5	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25℃), Note 2 I_F=20 mA

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	7.5	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN	3.0	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	9.5	10	10.5	KHz	
PWM Duty Ratio	Duty	5	--	100	%	

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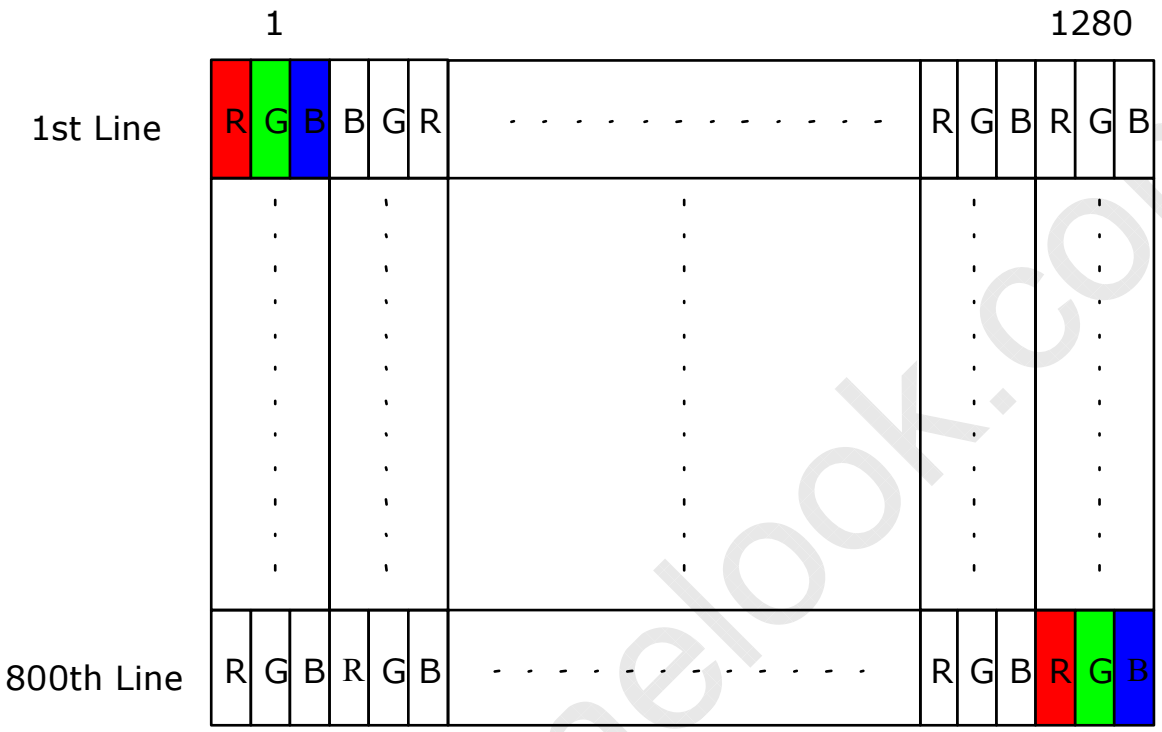
6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



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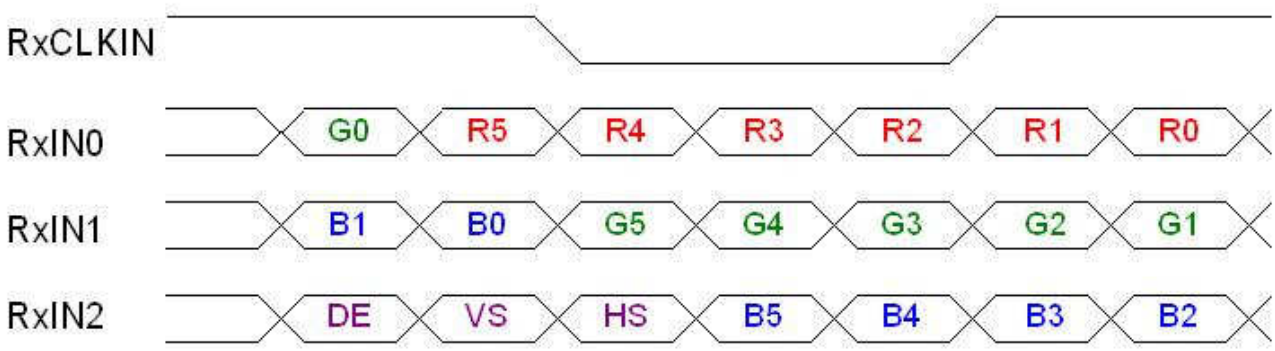
6.2 The input data format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

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6.3 Integration Interface and Pin Assignment

6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-030E-12 or compatible
Mating Housing/Part Number	IPEX 20453-030T-02 or compatible

6.3.2 Pin Assignment

Pin #	Signal Name	Signal Descr.	Pin #	Signal Name	Signal Descr.
1	PAID	Conn. Continuity Test	16	LCD_GND	LCD logic and driver ground
2	H_GND	High Speed Ground	17	HPD	HPD signal pin
3	Lane1_N	Comp Signal Link Lane 1	18	BL_GND	Backlight ground
4	Lane1_P	True Signal Link Lane 1	19	BL_GND	Backlight ground
5	H_GND	High Speed Ground	20	BL_GND	Backlight ground
6	Lane0_N	Comp Signal Lane 0	21	BL_GND	Backlight ground
7	Lane0_P	True Signal Link Lane 0	22	NC	No Connect
8	H_GND	High Speed Ground	23	BL_PWM_DIM	System PWM signal input
9	AUX_CH_P	True Signal Auxiliary Ch.	24	SMBUS_CLK	Backlight Control Clk
10	AUX_CH_N	Comp Signal Auxiliary Ch.	25	SMBUS_DATA	Backlight Control Data
11	H_GND	High Speed Ground	26	BL_PWR	Backlight power
12	LCD_VCC	LCD logic and driver power	27	BL_PWR	Backlight power
13	LCD_VCC	LCD logic and driver power	28	BL_PWR	Backlight power
14	BIST	LCD Panel Self Test Enable	29	BL_PWR	Backlight power
15	LCD_GND	LCD logic and driver ground	30	PAID	Conn. Continuity Test

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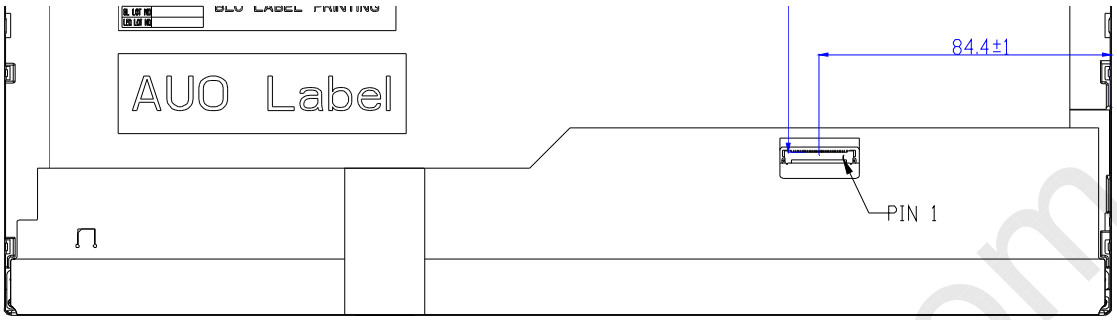
Note1: Start from right side
(Need to update to new drawing and connector location!!!!)



Note2: Input signals shall be low or High-impedance state when VDD is off.

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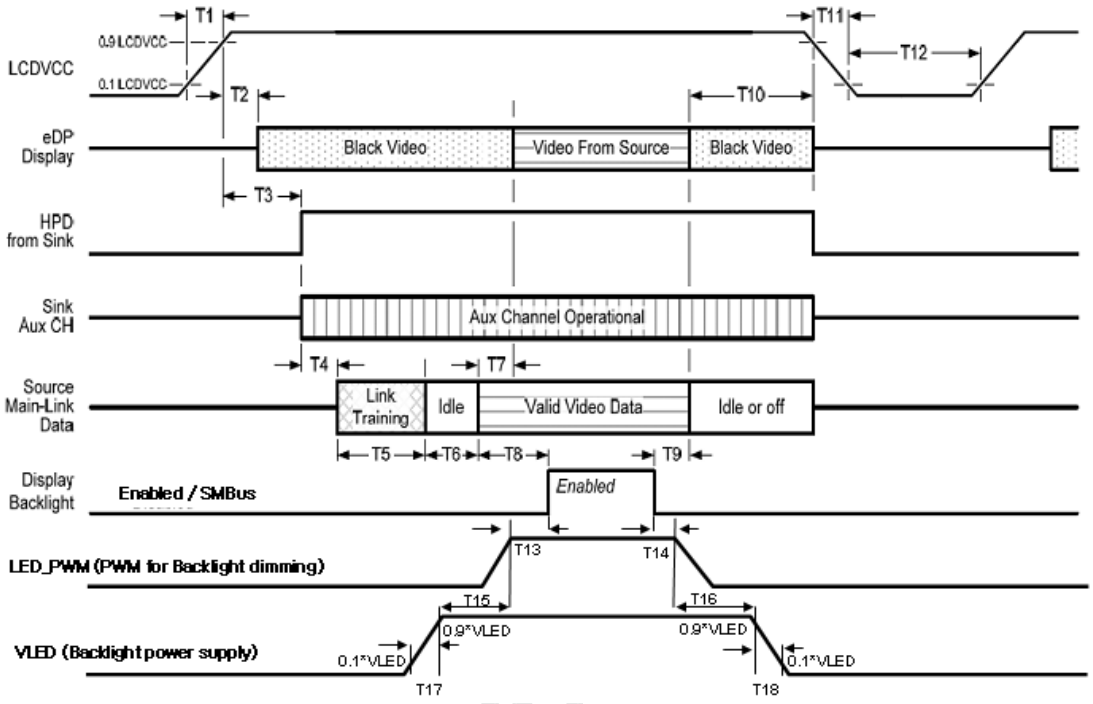
6.5 Power ON/OFF Sequence

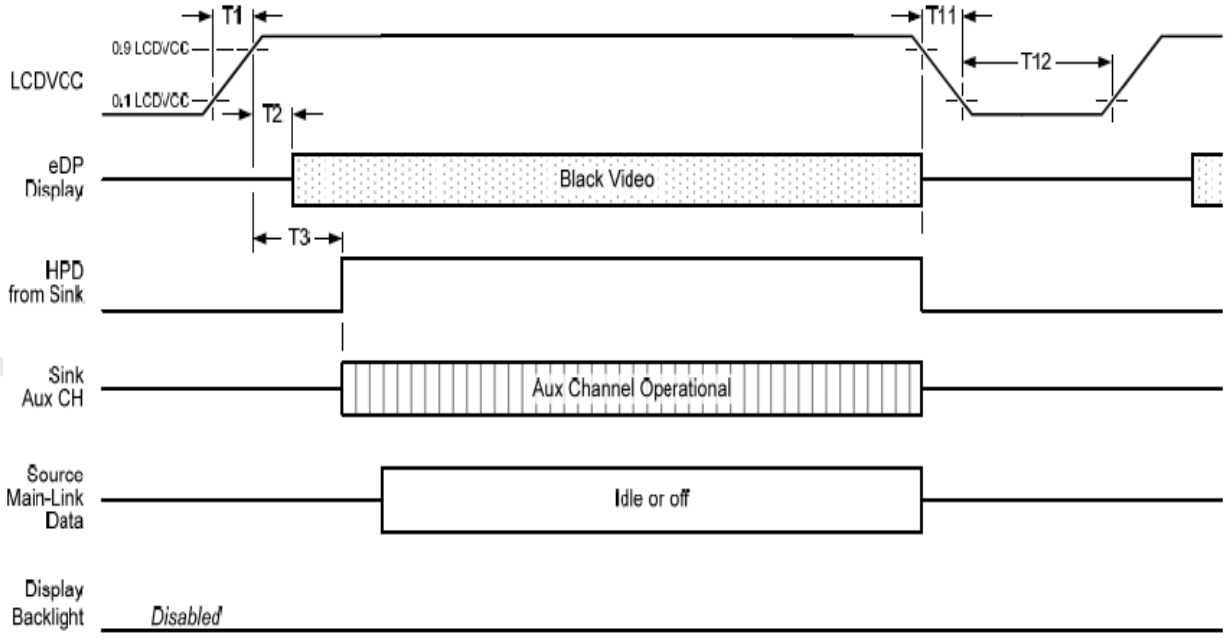
VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

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Display Port panel power sequence timing parameter:

Timing Parameter	Description	Reqd. By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	
T2	Delay from LCDVCC to black video generation	Sink	0ms	200ms	Prevents display noise until valid video data is received from the Source (see note 1 below)
T3	Delay from LCDVCC to HPD high	Sink	0ms	200ms	Sink Aux Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max allows Sink validate video data and timing
T8	Delay from valid video data from Source to backlight enable	Source	-	-	Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	Source must assure backlight is no longer illuminated (see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T11	Power rail fall time, 90% to 10%	Source	-	10ms	
T12	Power off time	Source	500ms	-	

Power Sequence Timing				
	Value			
Parameter	Min.(ms)	Typ.(ms)	Max.(ms)	Condition
T13	10	-	-	
T14	10	-	-	
T15	10	-	-	
T16	10	-	-	
T17	0.5	-	10	
T18	0	-	10	

Note 1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)
-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without

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causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port signal cable impedance request:

Signal cable impedance:
The variation of the cable impedance must be within 100ohms +/-15% from a system to a panel connector.

Parameter	Condition	Min.	Typ.	Max.	Unit
Cable impedance	System to panel connector	85	100	115	Ohm

LED on/off sequence is as follows. Interface signals are also shown in the chart.

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7. Vibration and Shock Test

7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G , Half sine pulse
- Frequency: 10 - 500Hz Sine wave
- Sweep: 30 Minutes each Axis (X, Y, Z)

7.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine pulse
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

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7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40℃, 95%RH, 300h	
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 65℃, 20%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 300h	
Thermal Shock Test	Ta=-40℃to 65℃, Duration at 30 min, 50 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

Note1: According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

Remark: MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

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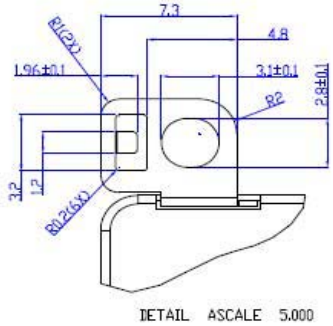
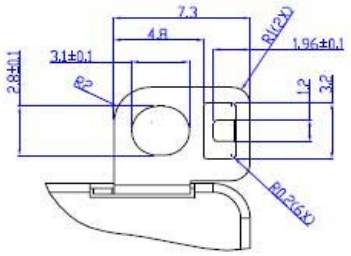
8. Mechanical Characteristics

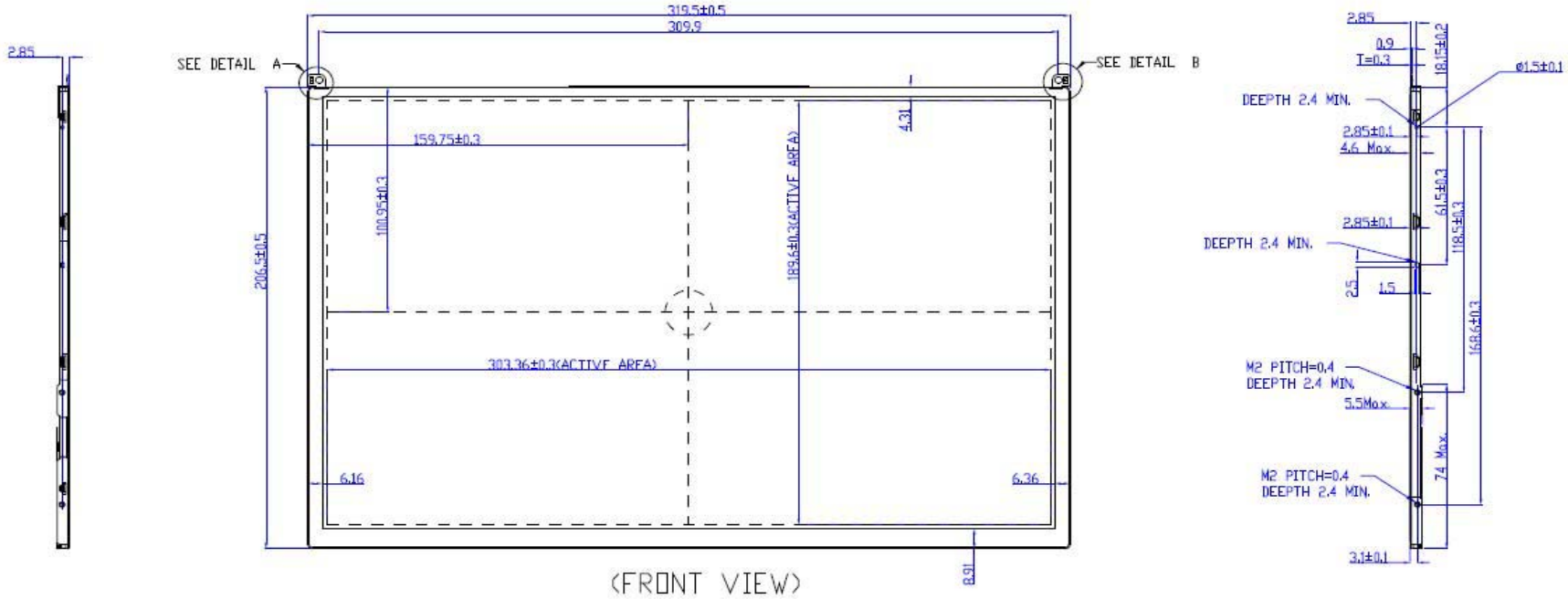
8.1 LCM Outline Dimension



DETAIL ASCALE 5.000



DETAIL B
SCALE 5.000



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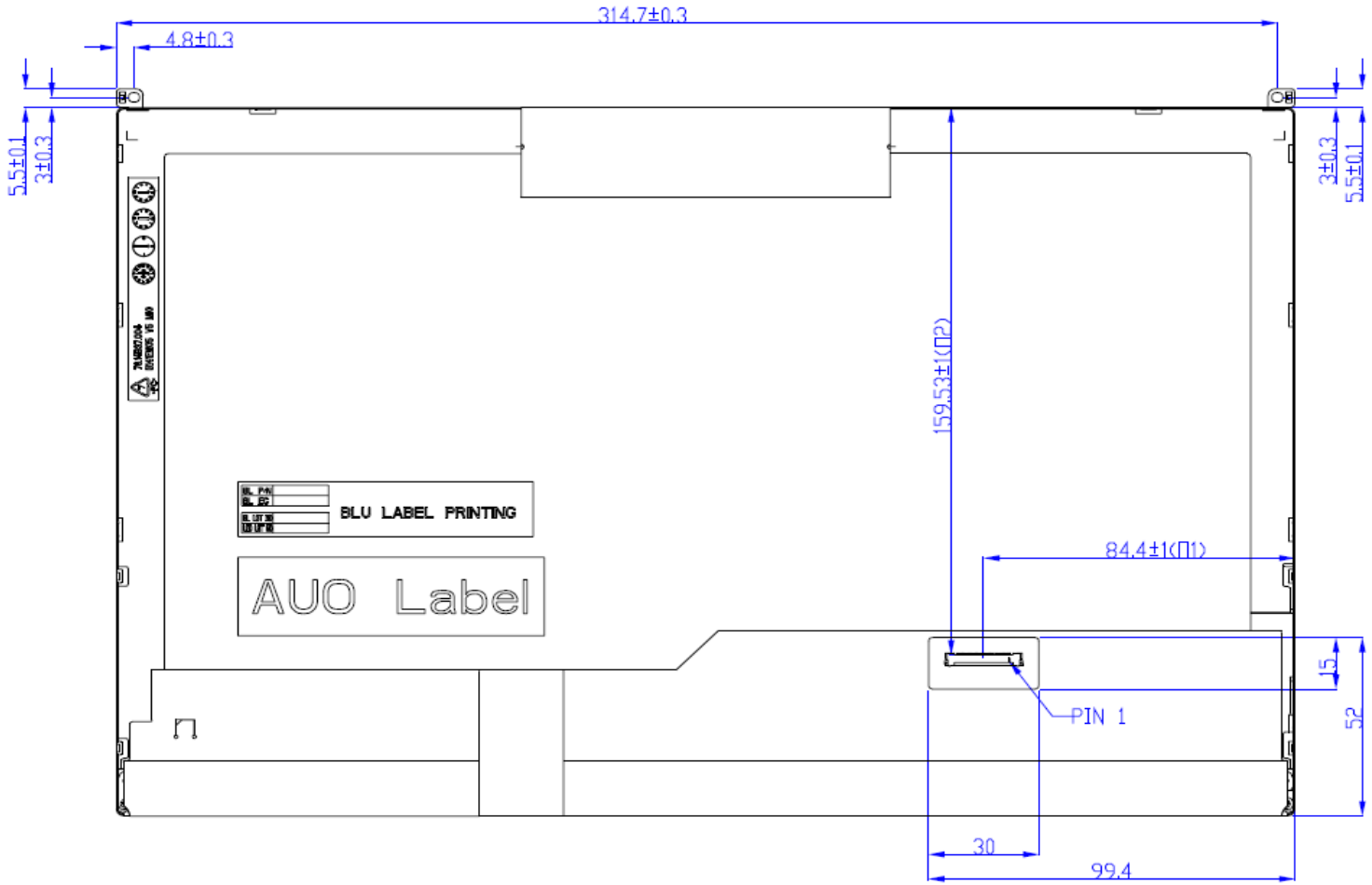

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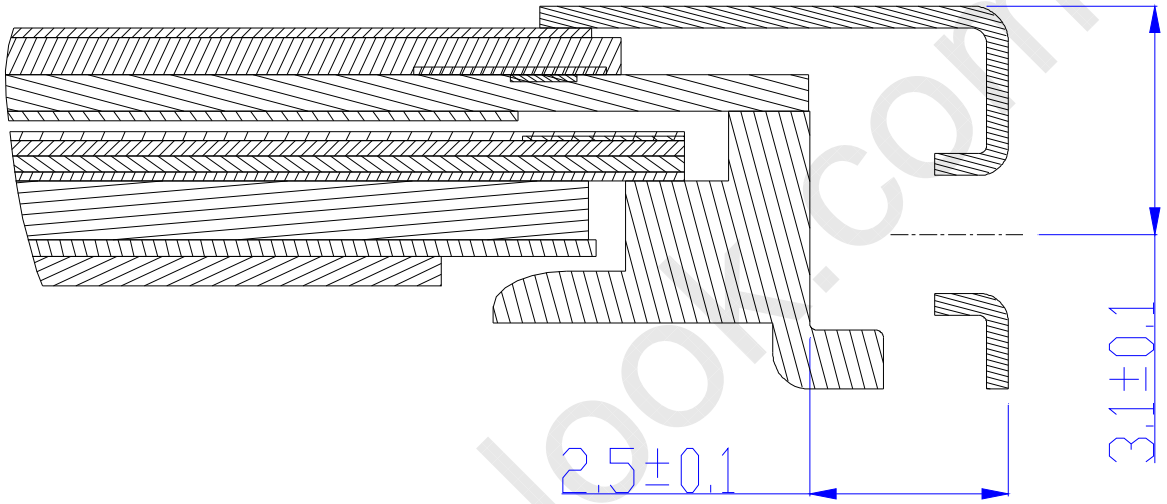
8.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface = 2.4 mm (See drawing)

Screw hole center location, from front surface = 3.1 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.5 kgf-cm



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9. Shipping and Package

9.1 Shipping Label Format

Revision Code (YYY) Tabel:

Build Name(s):	PPID Revision Code(s):
Sub System Test (SST) Working Sample (WS) ENG 2	X00, X01, X02, …, X0n
Product Test (PT) Engineering Sample (ES) ENG 3	X10, X11, X12, …, X1n
System Test (ST) Customer Sample (CS) ENG 4	X20, X21, X22, … X2n
X-Build (XB) Mass Production (MP) ENG 5	A00, A01, A02, … A0n

Update to Dell version Label fromat

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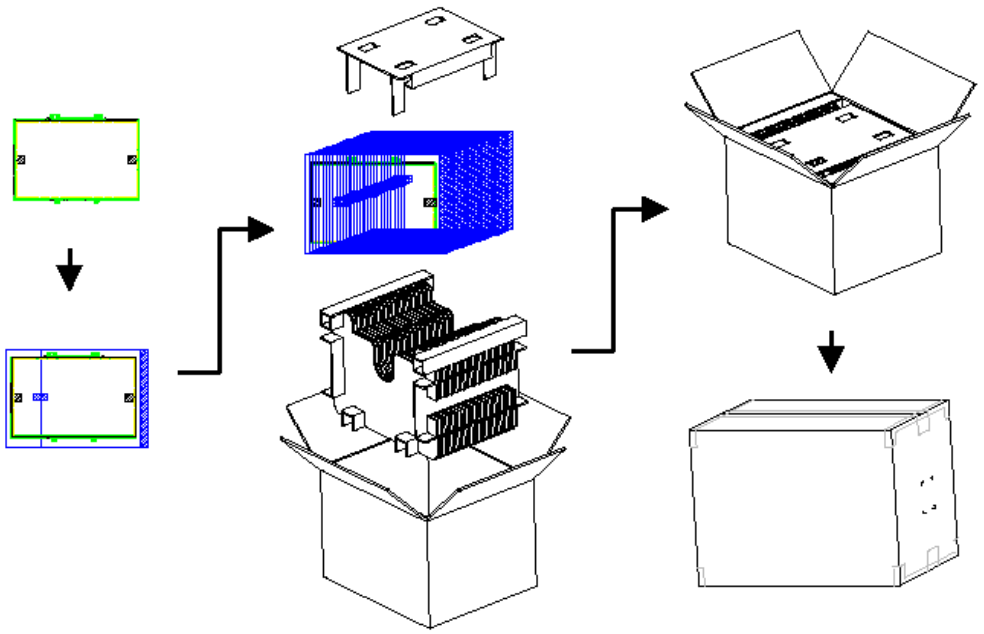
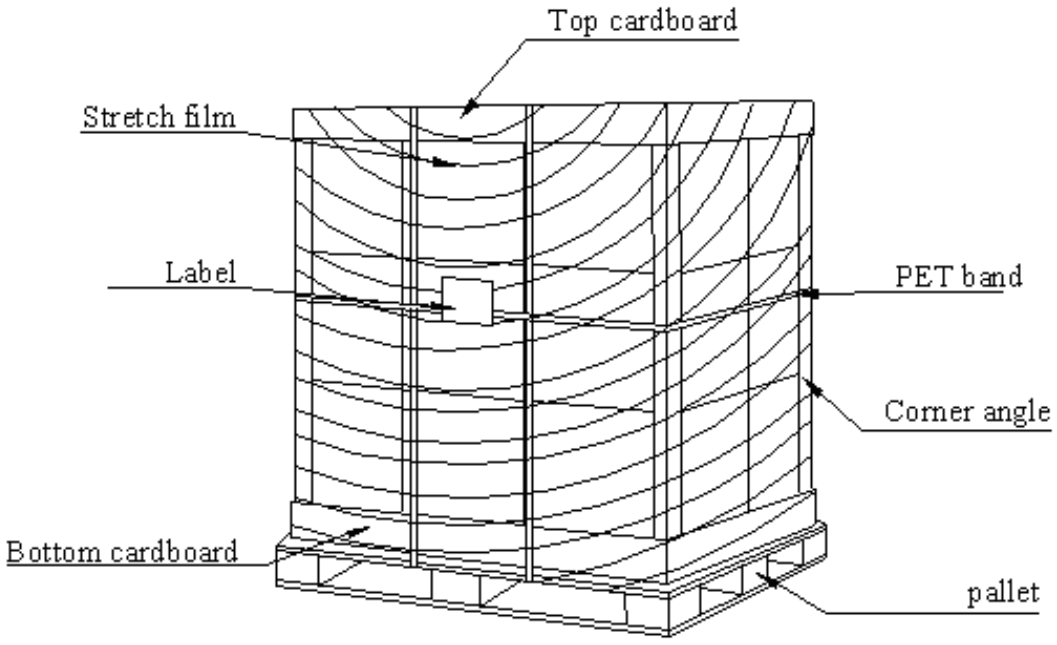
9.2 Carton package

The outside dimension of carton is 455 (L)mm x 380 (W)mm x 355 (H)mm



9.3 Shipping package of palletizing sequence



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10. Appendix: EDID description

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
Header	0	Header	00	00000000	0
	1	Header	FF	11111111	255
	2	Header	FF	11111111	255
	3	Header	FF	11111111	255
	4	Header	FF	11111111	255
	5	Header	FF	11111111	255
	6	Header	FF	11111111	255
	7	Header	00	00000000	0
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	06	00000110	6
	9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
	0A	Panel Supplier Reserved – Product Code	44	01000100	68
	0B	Panel Supplier Reserved – Product Code	55	01010101	85
	0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
	10	Week of manufacture	01	00000001	1
	11	Year of manufacture	14	00010100	20
	12	EDID structure version # = 1	01	00000001	1
	13	EDID revision # = 4	04	00000100	4
Display Parameters	14	Video I/P definition = Digital I/P (90 (6-bit) or A0 (8-Bit))	95	10010101	149
	15	Max H image size = ?? cm(Rounded to cm)	1E	00011110	30
	16	Max V image size = ?? cm(Rounded to cm)	13	00010011	19
	17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
	18	Feature support	02	00000010	2
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	C9	11001001	201
	1A	Blue/White Low bit (BxBy/WxWy)	31	00110001	49
	1B	Red X Rx = 0.???	9B	10011011	155
	1C	Red Y Ry = 0.???	59	01011001	89
	1D	Green X Rx = 0.???	52	01010010	82
	1E	Green Y Ry = 0.???	8F	10001111	143
	1F	Blue X Rx = 0.???	26	00100110	38
	20	Blue Y Ry = 0.???	23	00100011	35
	21	White X Rx = 0.???	4E	01001110	78
	22	White Y Ry = 0.???	55	01010101	85
Established Timings	23	Established timings 1 (00h if not used)	00	00000000	0
	24	Established timings 2 (00h if not used)	00	00000000	0
	25	Manufacturer’s timings (00h if not used)	00	00000000	0
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001	1
	27	Standard timing ID1 (01h if not used)	01	00000001	1
	28	Standard timing ID2 (01h if not used)	01	00000001	1

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	29	Standard timing ID2 (01h if not used)	01	00000001	1
	2A	Standard timing ID3 (01h if not used)	01	00000001	1
	2B	Standard timing ID3 (01h if not used)	01	00000001	1
	2C	Standard timing ID4 (01h if not used)	01	00000001	1
	2D	Standard timing ID4 (01h if not used)	01	00000001	1
	2E	Standard timing ID5 (01h if not used)	01	00000001	1
	2F	Standard timing ID5 (01h if not used)	01	00000001	1
	30	Standard timing ID6 (01h if not used)	01	00000001	1
	31	Standard timing ID6 (01h if not used)	01	00000001	1
	32	Standard timing ID7 (01h if not used)	01	00000001	1
	33	Standard timing ID7 (01h if not used)	01	00000001	1
	34	Standard timing ID8 (01h if not used)	01	00000001	1
	35	Standard timing ID8 (01h if not used)	01	00000001	1
Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	F4	11110100	244
	37	Pixel Clock/10,000 (MSB)	1A	00011010	26
	38	Horizontal Active = ???? pixels (lower 8 bits)	00	00000000	0
	39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	72	01110010	114
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
	3B	Vertical Active = ??? lines	20	00100000	32
	3C	Vertical Blanking (Tvbp) = ?? lines (DE Blanking typ. for DE only panels)	17	00010111	23
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
	3E	Horizontal Sync, Offset (Thfp) = ?? pixels	30	00110000	48
	3F	Horizontal Sync, Pulse Width = ??? pixels	20	00100000	32
	40	Vertical Sync, Offset (Tvfp) = ? lines Sync Width = ? lines	36	00110110	54
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	42	Horizontal Image Size =??? mm	2F	00101111	47
	43	Vertical image Size = ??? mm	BD	10111101	189
	44	Horizontal Image Size / Vertical image size	10	00010000	16
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
Timing Descripter #2 (=Timing Descripter #1)	48	Pixel Clock/10,000 (LSB)	ED	11101101	237
	49	Pixel Clock/10,000 (MSB)	11	00010001	17
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	00	00000000	0
	4B	Horizontal Blanking (Thbp) = xxxx pixels	72	01110010	114

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		(lower 8 bits)			
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000	80
	4D	Vertical Active = xxxx lines	20	00100000	32
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	17	00010111	23
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	30	00110000	48
	51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000	32
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	36	00110110	54
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
	54	Horizontal Image Size =xxx mm	2F	00101111	47
	55	Vertical image Size = xxx mm	BD	10111101	189
	56	Horizontal Image Size / Vertical image size	10	00010000	16
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, see VESA EDID Spec 1.3 Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] : The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see VESA EDID Spec 1.3 Bit[0] : See VESA EDID Spec 1.3 ==> fix=1A	1A	00011010	26
Timing Descripter #3 Dell specific information	5A	Flag	00	00000000	0
	5B	Flag	00	00000000	0
	5C	Flag	00	00000000	0
	5D	Data Type Tag: Alphanumeric Data String (ASCII) ==> fix=FE	FE	11111110	254
	5E	Flag	00	00000000	0
	5F	Dell P/N 1st Character	34	00110100	52
	60	Dell P/N 2nd Character	34	00110100	52
	61	Dell P/N 3rd Character	50	01010000	80
	62	Dell P/N 4th Character	36	00110110	54
	63	Dell P/N 5th Character	34	00110100	52
	64	**EDID Revision Bit[6:0] See charts below Bit[7] 0: X-rev, 1: A-rev**	80	10000000	128
	65	Manufacturer P/N	42	01000010	66
	66	Manufacturer P/N	31	00110001	49
	67	Manufacturer P/N	34	00110100	52
	68	Manufacturer P/N	31	00110001	49
	69	Manufacturer P/N	45	01000101	69
	6A	Manufacturer P/N	57	01010111	87
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	35	00110101	53
Timing Descripter #4	6C	Flag	00	00000000	0
	6D	Flag	00	00000000	0
	6E	Flag	00	00000000	0
	6F	Data Type Tag: Manufacturer Specified Data 00 ==>fix=00	00	00000000	0

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	70	Flag	00	00000000	0
	71	Color Management	00	00000000	0
	72	Panel Structure	41	01000001	65
	73	Frame Rate	21	00100001	33
	74	Light Controller Interface and Luminance	16	00010110	22
	75	Outdoor Features	00	00000000	0
	76	Multi-Media Features	00	00000000	0
	77	Multi-Media Features	00	00000000	0
	78	Special Features #1	00	00000000	0
	79	Special Features #2	09	00001001	9
	7A	Special Features #3	01	00000001	1
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	E8	11101000	232

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